

### REMARKS

Claims 1, 3-8, 10-12 and 14 are pending in the action, with claims 1, 5, 8 and 12 being independent. Claims 1, 3-8, 10-12 and 14 have been amended. Claim 15 is new. No new matter has been added.

Claims 1, 5, 8 and 12 are rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Applicant's admitted prior art (AAPA) in view of USP No. 6,078,532 to Rivers.

Claims 3-4, 6-7, 10-11 and 14 are rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over the AAPA in view of Rivers, and further in view of USP No. 6,154,746 to Berchtold.

Claims 1, 5, 8 and 12 are rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Applicant's admitted prior art (AAPA) in view of USP No. 5,588,130 to Fujishima.

Claims 3-4, 6-7, 10-11 and 14 are rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over the AAPA in view of Fujishima, and further in view of Berchtold.

The Applicant traverses these rejections. Reconsideration and allowance of the above-referenced application are respectfully requested in light of the following remarks.

### **Section 103(a) Rejections**

Claims 1, 5, 8 and 12 are rejected as allegedly being unpatentable over the AAPA in view of Rivers.

Claim 1, as amended, recites in part searching only a DRAM portion of a SRAM and DRAM lookup table if no routing information is found in a SRAM portion.

In the statement of rejection, the Examiner admits that the AAPA does not disclose the claimed SRAM and DRAM lookup table, and relies upon col. 2, lines 10-20 of Rivers to arrive at the claimed invention (page 2, item 2 of Office Action).

Referring to the cited section, Rivers describes a DRAM/SRAM cache system in which each data access directly obtains data only from the SRAM cache (2:11-13). In such a system, if the requested data does not reside in the SRAM cache, Rivers replaces a row of SRAM cache (e.g., least used) with a row of DRAM containing the desired data (2:13-16) so as to permit all data for a given request to be read directly from the SRAM cache (2:18-19). This loading

process is followed by searching the entire SRAM cache, including searching the new row in the SRAM cache that contains the loaded data from the DRAM. Thus, Rivers teaches away from the claimed invention, because Rivers searches and accesses all data directly from the SRAM cache, even in the presence of a cache miss. Rivers does not disclose or suggest searching only the DRAM if no routing information is found in the SRAM cache. For at least these reasons, claim 1, as amended, is allowable over the AAPA and Rivers, alone or in combination. Claims 3 and 4 depend on claim 1, and also are submitted to be allowable over the AAPA and Rivers for reasons discussed above with respect to claim 1.

Claim 5, as amended, recites in part accessing an SRAM portion of a routing table for routing information, and accessing only a DRAM portion of the routing table if no entry corresponding to the routing identification information is found in the SRAM portion.

However, as discussed *supra*, neither the AAPA nor Rivers, alone or in combination, disclose or suggest accessing only the DRAM when the requested data are not found in the SRAM. For at least these reasons, claim 5, as amended, is allowable over the AAPA and Rivers, alone or in combination. Claims 6 and 7 depend on claim 5, and also are submitted to be allowable over the AAPA and Rivers for reasons discussed above with respect to claim 5.

Claim 8, as amended, recites in part that a predetermined number of levels of a search of a SRAM and DRAM lookup table is stored in an SRAM portion, and a remaining number of levels of the search is stored in the DRAM portion.

In the statement of rejection, the Examiner admits that the combination of the AAPA and Rivers do not teach these limitations, and relies on col. 1 line 30 *et seq* and col. 15, line 15 *et seq* of Berchtold to arrive at the claimed invention (page 3, 1<sup>st</sup> ¶ of Office Action).

Berchtold discloses an index file structure for use in database management to provide quick and efficient associative access to a table's record (1:33-35). To facilitate an efficient in-page search for matching objects, the index file structure is configured using a B-Tree structure consisting of a root node and many levels of nodes branching from the root node (1:35-36), and bisection or interval search algorithms are applied to the B-Tree structure (15:15-17).

However, Berchtold does not provide disclosure in which the bisection or interval search algorithm includes, for example, a number of search levels stored in a SRAM with the remaining search levels being stored in a DRAM. While Berchtold teaches the application of a bisection or

interval search algorithm in a database management environment to improve performance of query processing, such search algorithms could still be implemented in a wide variety of fashions, and Berchtold's objective can still be accomplished without the express teaching of storing search levels in a SRAM and DRAM.

In contrast, the claimed lookup table can include, for example, an interval bisection or binary tree structure that can be divided into one or more search levels (e.g., levels 701-704 of FIG. 7) in which the top level(s) of the structure is(are) stored in a SRAM and the remaining level(s) is(are) stored in a DRAM (e.g., page 7, lines 4-9 and lines 12-16 of the specification).

For at least these reasons, claim 8, as amended, is allowable over the AAPA, Rivers and Berchtold, alone or in combination. Claims 10 and 11 depend on claim 8, and also are submitted to be allowable over the proposed combination of the AAPA, Rivers and Berchtold for reasons discussed above with respect to claim 8.

Claim 12, as amended, recites in part that a first portion of a search of a routing table is conducted in a SRAM cache and a second portion is conducted in a DRAM portion, wherein only the second portion of the search in the DRAM portion is conducted only if no routing information is found in the SRAM portion.

However, as discussed *supra*, neither the AAPA nor Rivers, alone or in combination, disclose or suggest searching only the DRAM when the requested data are not found in the SRAM. For at least these reasons, claim 12, as amended, is allowable over the AAPA and Rivers, alone or in combination. Claim 14 depends on claim 12, and also is submitted to be allowable over the AAPA and Rivers for reasons discussed above with respect to claim 14.

### **Section 103(a) Rejections**

Claims 1, 5, 8 and 12 are rejected as allegedly being unpatentable over the AAPA in view of Fujishima.

Claim 1, as amended, recites in part searching only a DRAM portion of a SRAM and DRAM lookup table if no routing information is found in a SRAM portion.

In the statement of rejection, the Examiner admits that the AAPA does not disclose using both DRAM and SRAM in a lookup table, and relies upon col. 8, line 5 *et seq* of Fujishima arrive at the claimed invention (page 3, item 4 of Office Action).

Fujishima teaches using a plurality of static type memory cells as a second memory cell (4:59-62). Utilizing the second memory cell as cache memory, access is made to the second memory cell prior to determination of a cache hit or cache miss (5:66-6:3), and data is extracted from the second memory cell (6:3-5). When cache miss occurs, data extracted from the static type memory cells (i.e., SRAM) is ignored (6:7-9).

Therefore, similar to the deficiencies found in Rivers, Fujishima also searches the static type memory cells even in the presence of a cache miss. Fujishima does not teach or suggest searching only the dynamic type memory cells if a particular data is not found in the static type memory cells.

For at least these reasons, claim 1, as amended, is allowable over the AAPA and Fujishima, alone or in combination. Claims 3 and 4 depend on claim 1, and also are submitted to be allowable over the AAPA and Fujishima for reasons discussed above with respect to claim 1.

Claim 5, as amended, recites in part accessing an SRAM portion of a routing table for routing information, and accessing only a DRAM portion of the routing table if no entry corresponding to the routing identification information is found in the SRAM portion.

However, as discussed *supra*, neither the AAPA nor Fujishima, alone or in combination, disclose or suggest accessing only the DRAM when the requested data are not found in the SRAM. For at least these reasons, claim 5, as amended, is allowable over the AAPA and Fujishima, alone or in combination. Claims 6 and 7 depend on claim 5, and also are submitted to be allowable over the AAPA and Fujishima for reasons discussed above with respect to claim 5.

Claim 8, as amended, recites in part that a predetermined number of levels of a search of a SRAM and DRAM lookup table is stored in an SRAM portion, and a remaining number of levels of the search is stored in the DRAM portion.

In the statement of rejection, the Examiner admits that the combination of the AAPA and Fujishima do not teach searching the claimed lookup table using interval bisection or binary tree search, and relies on col. 1 line 30 *et seq* and col. 15, line 15 *et seq* of Berchtold to arrive at the claimed invention (page 4, 1<sup>st</sup> ¶ of Office Action).

However, as discussed *supra*, Berchtold does not provide disclosure in which the bisection or interval search algorithm includes, for example, a number of search levels stored in a SRAM with the remaining search levels being stored in a DRAM. While Berchtold teaches the

application of a bisection or interval search algorithm in a database management environment to improve performance of query processing, such search algorithms could still be implemented in a wide variety of fashions, and Berchtold's objective can still be accomplished without the express teaching of storing search levels in a SRAM and DRAM.

For at least these reasons, claim 8, as amended, is allowable over the AAPA, Fujishima and Berchtold, alone or in combination. Claims 10 and 11 depend on claim 8, and also are submitted to be allowable over the proposed combination of the AAPA, Fujishima and Berchtold for reasons discussed above with respect to claim 8.

Claim 12, as amended, recites in part that a first portion of a search of a routing table is conducted in a SRAM cache and a second portion is conducted in a DRAM portion, wherein only the second portion of the search in the DRAM portion is conducted only if no routing information is found in the SRAM portion.

However, as discussed *supra*, neither the AAPA nor Fujishima, alone or in combination, disclose or suggest searching only the DRAM when the requested data are not found in the SRAM. For at least these reasons, claim 12, as amended, is allowable over the AAPA and Fujishima, alone or in combination. Claim 14 depends on claim 12, and also is submitted to be allowable over the AAPA and Fujishima for reasons discussed above with respect to claim 14.

### Conclusion

The Applicant respectfully requests that all pending claims be allowed.

By responding in the foregoing remarks only to particular positions taken by the Examiner, the Applicant does not acquiesce with other positions that have not been explicitly addressed. In addition, Applicant's arguments for the patentability of a claim should not be understood as implying that no other reasons for the patentability of that claim exist.

For all of the reasons set forth above, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicant's attorney at the telephone number shown below.

The three-month extension of time fee in the amount of \$1020.00 is being paid concurrently herewith on the Electronic Filing System (EFS) by way of Deposit Account authorization. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: \_\_\_\_\_

2/7/07



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